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Half bridge converter
DC balance with current signal injection

December 2012

Control methods in pulse width modulated converters

The half bridge converter has been around for many years. It has a good utilization of magnetic components and can be a quite efficient and compact power converter.

The half bridge converter (figure 3) is one of the buck derived converters. However, the half bridge converter seems to be less popular than the rest of the buck derived converter family. The reason could be an inherent control problem of the half bridge which we will study in this article.

But first, let us talk a little about basic control methods of pulse width modulated converters.
In pulse width modulated converters the active switch is turned on and off at a fixed (high) frequency and the pulse width – or the duty cycle – of the switch's on-time is controlled by a feedback signal which is derived by linear amplification and filtering of the error signal (the difference between actual output voltage and desired output voltage). If, for some reason, the output voltage is lower than desired, the duty cycle must be adjusted up, to get the output voltage back on the desired value.

The oldest control method is known as "Voltage Mode Control" (VMC). With VMC, the pulse width is determined by comparing the slowly varying feedback signal to a fixed modulator ramp, as illustrated in figure 1.
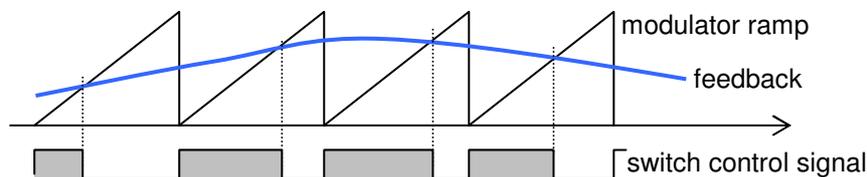
Figure 1   Voltage mode control

Around 1975 a new control method called "Current Mode Control" (CMC) started to be used in pulse width modulated converters, and since then it has become still more popular. The switch is turned on by a clock signal and turned off when the current in the inductor or the switch reaches a value determined by the feedback signal. This is shown in figure 2.
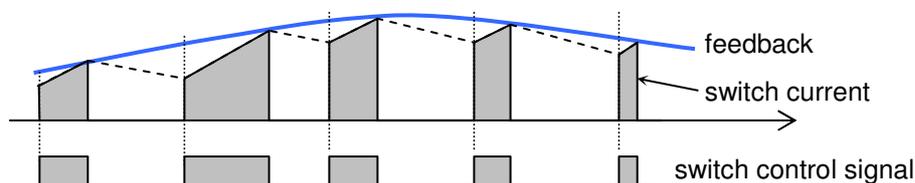
Figure 2   Current mode control

Many power supply designers today prefer CMC over VMC due to the following advantages:

1. A power stage with VMC has two complex poles. A power stage with CMC has only one real pole. This makes it simpler to close the feedback loop with CMC and most often with better results.
2. CMC has an inherent current limiter since current is measured and controlled from pulse to pulse.
3. CMC does not show the abrupt change in power stage gain on the boundary to discontinuous current as VMC does.

However, a disadvantage with CMC is that it becomes unstable when the duty cycle is above 50%. This instability, called subharmonic oscillation, has nothing to do with the outer feedback loop. It is inherent in the current mode controller itself (ref. 1 + 2).

The normal way to prevent subharmonic oscillation is to add a ramp signal, typically a fraction of the oscillator ramp, to the current signal, before comparing it to the feedback signal. This technique is often referred to as "slope compensation". More or less ramp can be used for slope compensation. It is important to note that CMC with slope compensation is really a combination of pure VMC and pure CMC, so the more slope compensation you use, the more you lose the mentioned three benefits of CMC. Too little ramp does not prevent subharmonic instability. More ramp than necessary can still work fine. But with slope compensation, a high frequency pole returns into the power stage gain, current limit becomes less accurate, and loop gain again experiences an abrupt change on the boundary to discontinuous current mode.

Voltage mode and current mode control can be used in all three basic topologies: buck, boost, and buck-boost and their derived topologies, except in the half bridge where VMC is the only possible control method. If you read on, you will see why, and you will also see that it is not completely true.

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page 2 of 11

Half bridge converter
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Half bridge and control strategies

It is known – by some designers at least – that the half bridge can only be controlled by Voltage Mode Control (VMC) or "Duty Cycle Control" as I prefer to name it.

Figure 3 shows a half bridge converter with its basic regulation characteristics and waveforms.

In the half bridge the two switches must run with the same pulse width, so that the midpoint between capacitors C1 and C2 will be at half of the input DC voltage.

If we try to use CMC in a half bridge, to gain the benefits of CMC, the midpoint voltage will tilt to one of two sides, either up or down. This will cause pulse width asymmetry which tends to increase the voltage imbalance. Many power supply designers are aware of that fact.

However, not many designers know that you can inject a limited amount of current signal on top of the VMC pulse-width-modulator ramp, and still maintain voltage balance in the half bridge.

But why should you do that?
Because it turns out that just a tiny amount of current signal injection can completely change the undesirable properties of the VMC loop towards the attractive properties achievable with CMC. This makes the half bridge more attractive than many designers think.

In general, CMC with slope compensation is always referred to as Current Mode Control, even though it is really a combination of VMC and CMC: the pulse width is influenced by the sum of a modulator ramp (VMC) and an injected current signal (CMC). For power supplies controlled by CMC the current signal is usually weighted high. For VMC there is usually only a ramp and no current signal. But any weighting between ramp and current signal can be chosen in the pulse width modulator.

A good question is:
How much current signal injection can be allowed on top of the modulator ramp in a half bridge, before the DC balance tilts? I do not think that question has ever been answered.

In this paper I will derive an expression for the maximum allowed current signal injection in a half bridge. In the end it turns out to be much simpler than anticipated during the derivation. This expression is now inserted in my half bridge feedback loop calculator to warn me if I go too far towards CMC.

$$Vo = \frac{1}{2} \cdot \frac{ns}{np} \cdot \delta \cdot Vin$$

$$\max \delta = 1$$
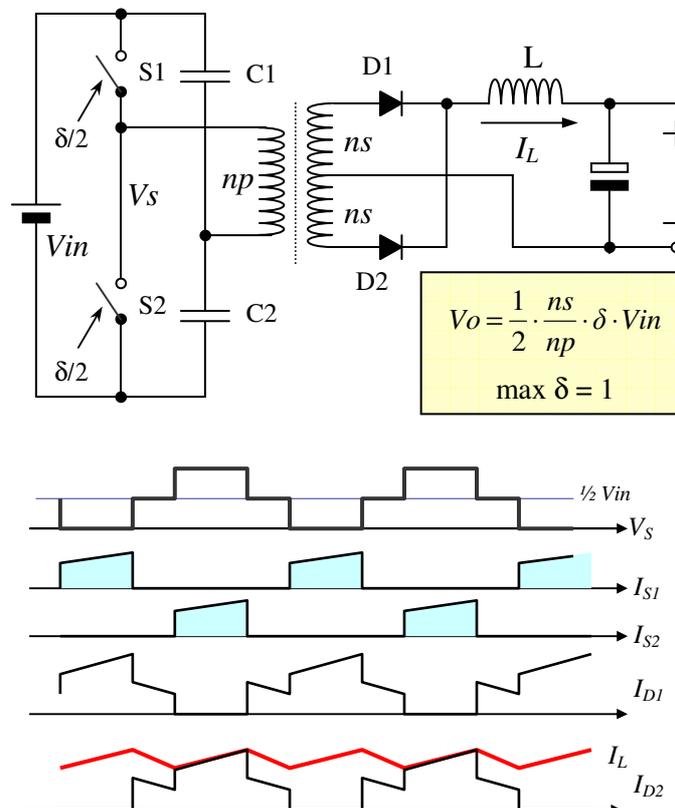
Figure 3   Half bridge with voltage and current waveforms

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Control of the basic half bridge

Figure 4 depicts the simplest possible half bridge. It has no transformer, i.e. no galvanic separation between input and output.

All components are assumed to be ideal, and the two capacitors are so large that no significant switching frequency voltage appears in the midpoint.

First we will study the situation where the two switches are controlled by pure CMC: The switches are turned on alternately by a fixed frequency clock generator. They are turned off when the inductor current I_L reaches a certain value, determined by a feedback signal.
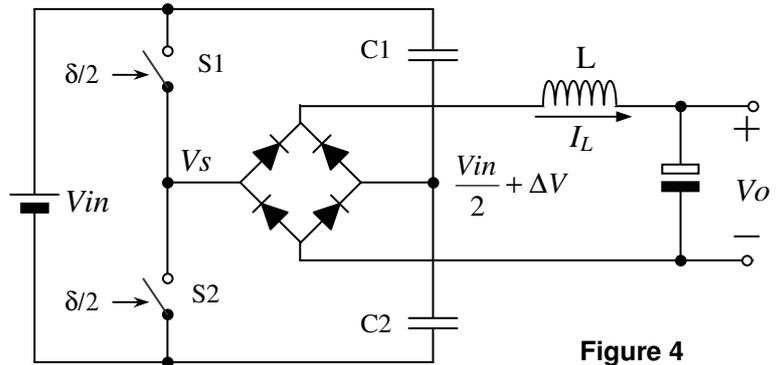
Figure 4
Basic half bridge

The voltage in the capacitor midpoint is assumed to be half of the input voltage + a voltage error ΔV. Such a voltage error must converge towards zero, otherwise we cannot control the converter.

Figure 5: The dotted lines show the inductor current and switch voltage when the half bridge is in balance: $\Delta V = 0$. The solid lines are the actual inductor current and switch voltage.
The hatched areas are the current pulses in switch S1 and S2 respectively.
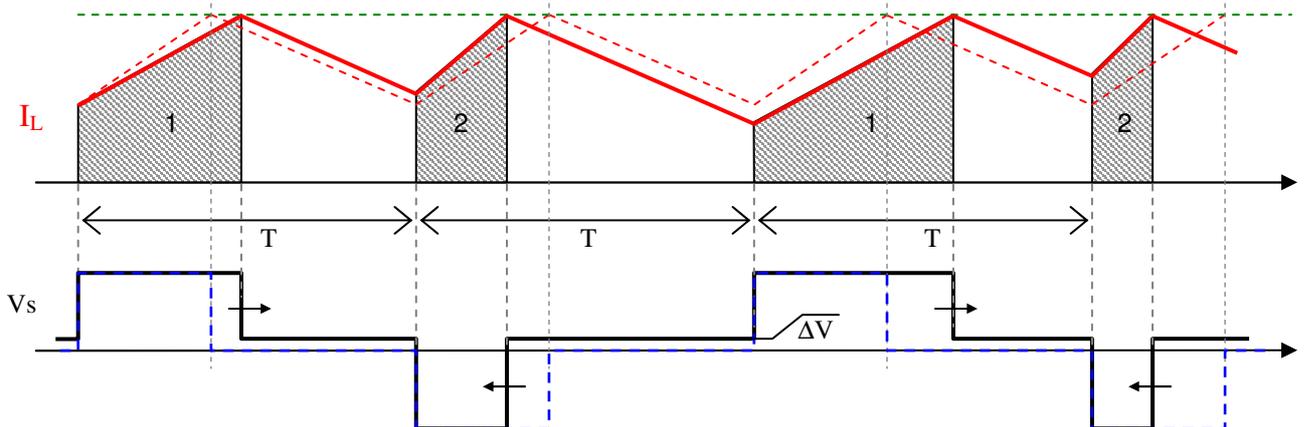
Figure 5 Basic half bridge with CMC

The up-slopes of inductor current are influenced by ΔV, the downslopes are constant, because V_o is constant.
It is evident from this drawing why a half bridge cannot be controlled by CMC. The average current through S1 keeps rising, the average current through S2 keeps falling. The average current into the capacitor midpoint is the difference between these two switch currents. Therefore ΔV, which was assumed to be positive, will rise faster and faster, increasing the initial imbalance.

With VMC or Duty Cycle Control, the duty cycle is constant for many cycles and independent on peak current, opposite to CMC. Half bridge converters are usually controlled by VMC which has no DC balance problem. Let's verify this by looking at the simple half bridge with VMC.

Figure 6 shows the situation with VMC. The downslopes are still constant and identical for the two half periods, proportional only to V_o/L. The up-slopes are alternately steeper and less steep than in the balanced situation. The inductor current is disturbed but returns to the initial value after a full cycle.
It is also evident from figure 6 that if $\Delta V > 0$, the average current in S1 and S2 are still identical (hatched areas of 1 and 2 are the same because areas of triangles above hatched areas are the same). Hence, the imbalance does not cause any net DC current into the capacitor midpoint. So in the ideal case any imbalance will persist. It will neither increase nor decrease in time. In a practical case it will of course decrease towards zero due to resistive effects.

This was a bit of a surprise to me. It means that in the ideal case, the VMC controlled half bridge is still on the boundary between stability and instability. Any tiny addition of current signal injection into the pulse width modulator will cause it to tilt immediately.

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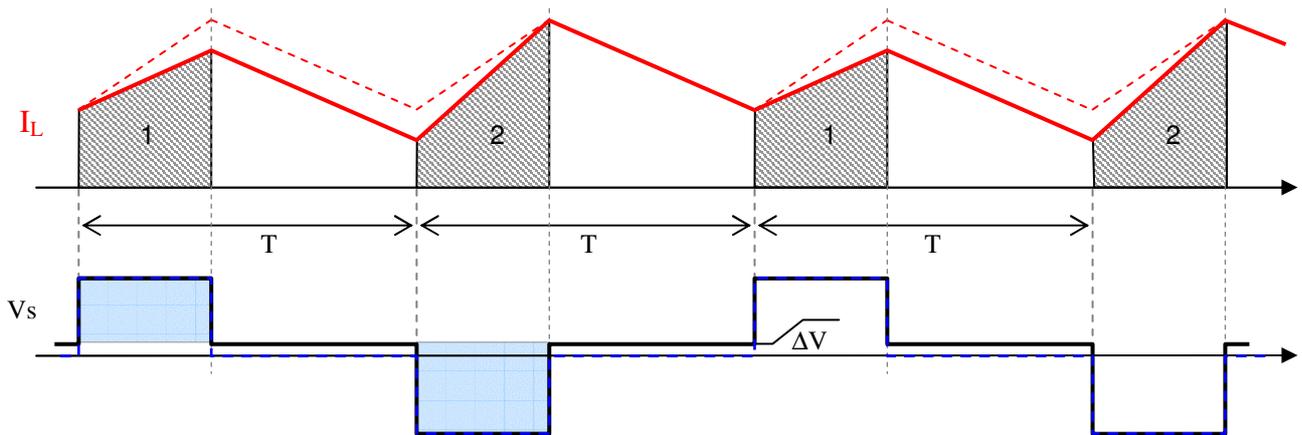
Figure 6 Basic half bridge with VMC

Compared to the real transformer coupled half bridge, we have made a crucial simplification: we have neglected the magnetizing inductance L_m of the transformer. In the simplified model of figure 4 the magnetizing inductance can be inserted horizontally in the diagonal of the bridge rectifier. L_m will be exposed to the blue hatched voltage pulses in figure 6. Since the area of these pulses are different, a current will start flowing to the left in L_m, pulling current out of the capacitor midpoint. Thus the midpoint voltage will go down, ΔV will get smaller. But it will just be the start of a ringing between $\frac{1}{2}V_{in} + \Delta V$ and $\frac{1}{2}V_{in} - \Delta V$ at the (low) resonance frequency between L_m and $C1+C2$. In the ideal case, the half bridge is still on the boundary between stability and instability. The ringing will persist, and any tiny injection of <u>inductor</u> current into the pulse width modulator will cause the ringing to grow exponentially.

Until now, all our studies have revealed the disappointing result that the half bridge converter can only be controlled by pure Duty Cycle Control. This agrees with the well established opinion among SMPS designers.
The next chapter will explain why it is not completely true.

Half bridge with current signal injection

Usually we measure current in the primary winding or in the two switches alternately because it is easily accessible there. And this makes a lot of difference, compared to measuring the inductor current.
The difference is magnetizing current I_m which is non-zero, as long as there is a voltage imbalance ΔV.
From figure 7 we see that when S1 is on, $I_p = -I_L + I_m$. When S2 is on, $I_p = I_L + I_m$. So alternately the magnetizing current adds to and subtracts from the inductor current.
For regulation, the sensed alternating current is rectified, shown with the small bridge symbol in figure 7. The current signal V_I is added to a voltage ramp V_{pp}, the sum is compared to a variable DC feedback voltage by a comparator, to form duty cycle modulated control pulses which are alternately fed to the two switches.

For a given current signal V_I we will now try to find the amount of ramp signal V_{pp} which will keep an imbalance ΔV unchanged from cycle to cycle. We call this situation "Critical Stability".

Having found this value, we know that if less ramp is used, ΔV will grow. If more ramp is used, ΔV will decay towards zero and the system will be stable.

Pulse width modulator
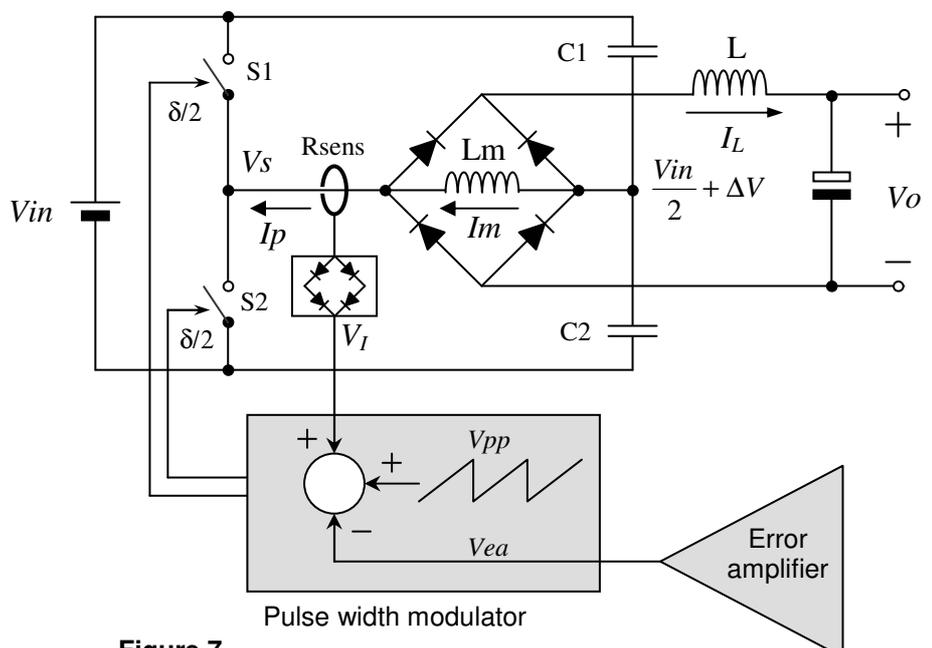
Figure 7
Transformer coupled half bridge with pulse width modulator

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According to figure 7, the width of the control pulses are determined by the sign of $((V_I + Vpp) - Vea)$ which is the same as $(V_I - (Vea - Vpp))$. So instead of adding a positive slope to the current signal and compare it to Vea, we can just as well subtract the inverse slope from Vea and compare this to the current signal V_I. In this way it is easier to draw the sketch in figure 8, which illustrates what we need to see.

We will assume that Lm is large and the ripple in Im is small.
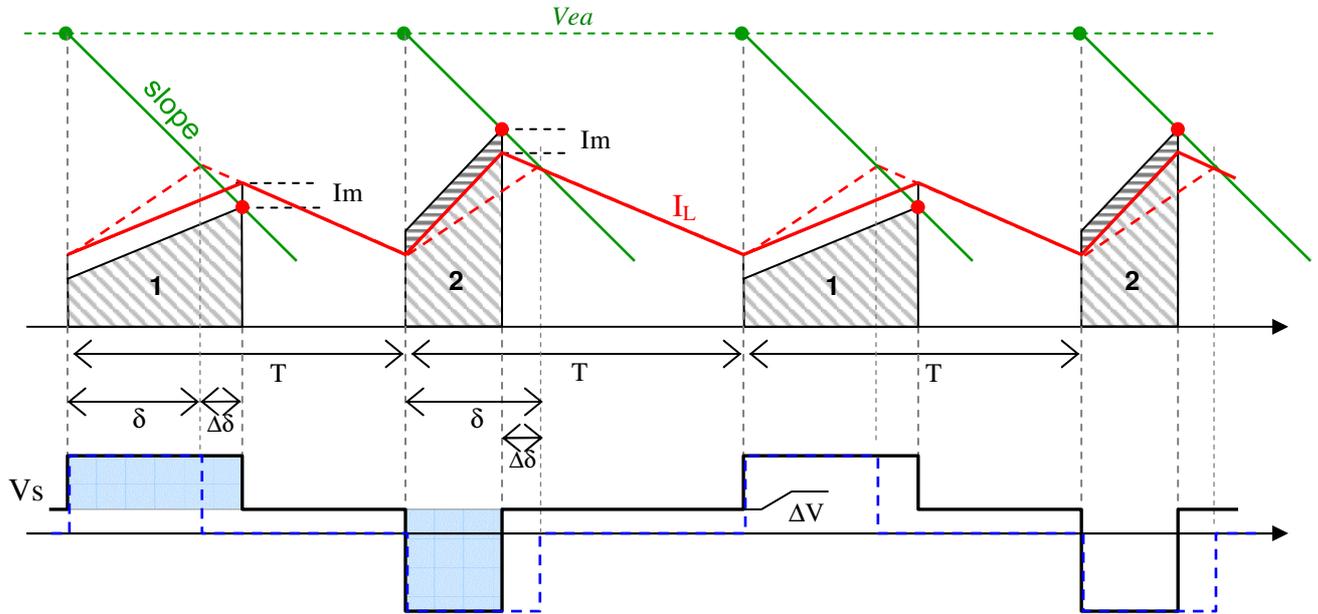
Figure 8 Critical stability situation

Figure 8 represents the critical stability situation.

The upper part of figure 8 shows currents, the lower part shows voltages. The dashed triangle wave is inductor current with perfect balance, the solid triangle is actual inductor current, influenced by ΔV. Hatched areas 1 and 2 are currents in S1 and S2 respectively. In area 1 the switch current is inductor current minus Im, in area 2 the switch current is inductor current + Im.

Two simple physical requirements in figure 8 must be met:
1) The two hatched current areas 1 and 2 must be equal. Only then will we have a net current flow of zero into the capacitor midpoint, and only then will an imbalance ΔV be unchanged from cycle to cycle.
2) The two hatched voltage areas must be equal because average voltage over Lm must be zero.

The negative control-slope always starts on the same level Vea with the clock interval T. When the slope intersects the switch current, the pulse is terminated, this event is marked with solid ball points. From a graphical point of view, this slope is exactly what is needed to maintain critical stability, i.e. ΔV which does not change from cycle to cycle.
If we use less slope and adjust Vea down until pulse 1 is terminated at the same instant, then pulse 2 will be terminated earlier, which reduces the area of pulse 2. That will push a net current into the capacitor midpoint and increase ΔV. If we use a higher slope, the two pulses will tend to have more equal width, which pulls a net current out of the capacitor midpoint and reduces ΔV.

Mathematical solution

The graphical solution to the problem in figure 8 is not very usable. We need to go through some algebra to find a mathematical expression which can be put into a calculator.

Assuming that the offset ΔV from balance is small (small signal approximation and linearization), the two deviations in duty cycle $\Delta\delta$ will be equal, one is positive, the other is negative.

The slope for critical stability can be found in figure 8 by studying the current and time difference between pulse 1 and 2, relative to the balanced situation.

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$$\text{slope} = \frac{\Delta y}{\Delta x} = \frac{\hat{I}_{L2} + \text{Im} - (\hat{I}_{L1} - \text{Im})}{2 \cdot \Delta \delta \cdot T} = \frac{2 \cdot \text{Im} + (\hat{I}_{L2} - \hat{I}_{L1})}{2 \cdot \Delta \delta \cdot T} \qquad (1)$$

where $\hat{I}_{L1}$ and $\hat{I}_{L2}$ are the peak inductor currents in pulse 1 and 2 respectively and T is the clock period.

To calculate the slope we must first find the three quantities: $\Delta \delta$, $\hat{I}_{L2} - \hat{I}_{L1}$ and Im expressed in terms of ΔV. In these calculations I will think of the slope as a current, not a voltage. Then, when we are finished we will translate it to a ramp voltage via the factor R_{sens}.

Calculation of duty cycle deviation $\Delta \delta$:

Average voltage over L_m is zero $\Rightarrow$ $\qquad (\delta + \Delta \delta) \cdot \left(\dfrac{\text{Vin}}{2} - \Delta V \right) = (\delta - \Delta \delta) \cdot \left(\dfrac{\text{Vin}}{2} + \Delta V \right)$ $\qquad (2)$

After multiplying out the brackets and solving for $\Delta \delta$ we get $\qquad \Delta \delta = 2 \cdot \delta \cdot \dfrac{\Delta V}{\text{Vin}}$ $\qquad (3)$

Calculation of $\hat{I}_{L2} - \hat{I}_{L1}$:

Here we need to use an approximation. Simulations have shown that when there is a voltage imbalance ΔV, this influences the peak inductor current but hardly the valley inductor current I_{Lmin}. It is not 100% correct but still a good approximation. Why it is so can be deduced from figure 8: the high pulses are terminated earlier so the current downslopes tends to follow the same trace and end at the same valley current. Therefore the difference between peak currents is nearly the same as difference between inductor ripple current during period 1 and 2:

$$\hat{I}_{L2} - \hat{I}_{L1} \approx I_{Lpp2} - I_{Lpp1} \qquad (4)$$

The inductor ripple currents are easy to express during the on-time. In the balanced situation it is

$$I_{Lpp} = \frac{\delta \cdot T}{L} \cdot \left(\frac{\text{Vin}}{2} - \text{Vo} \right) \qquad (5)$$

For ripple currents with voltage imbalance we add small signal terms in time and voltage:

$$I_{Lpp2} - I_{Lpp1} = \frac{T}{L} \cdot \left[(\delta - \Delta \delta) \cdot \left(\frac{\text{Vin}}{2} + \Delta V - \text{Vo} \right) - (\delta + \Delta \delta) \cdot \left(\frac{\text{Vin}}{2} - \Delta V - \text{Vo} \right) \right] \qquad (6)$$

This simplifies after some algebra to $\qquad I_{Lpp2} - I_{Lpp1} = 2 \cdot \dfrac{T}{L} \cdot \delta^2 \cdot \Delta V$ $\qquad (7)$

We have inserted (3) and used that $\qquad \delta = \dfrac{\text{Vo}}{0.5 \cdot \text{Vin}}$ $\qquad (8)$

For the calculation of Im we must first find the average <u>inductor</u> current during on-times 1 and 2 (figure 8): Let's define $I_{L1} = av(I_L)$ during pulse 1 and $I_{L2} = av(I_L)$ during pulse 2. Then complete average inductor current $I_L = P/\text{Vo} = \frac{1}{2}(I_{L1} + I_{L2})$,

where P is power, again under the approximation that valley inductor current I_{Lmin} is identical for the two half cycles.

$$I_{L1} = I_{Lmin} + \frac{1}{2} \cdot I_{Lpp1} \qquad\qquad I_{L2} = I_{Lmin} + \frac{1}{2} \cdot I_{Lpp2} \qquad (9)$$

Since I_{L1} and I_{L2} are spaced symmetrically around I_L with distance $I_{L2} - I_{L1}$, we can write by using (9):

$$I_{L1} = I_L - \frac{1}{2} \cdot (I_{L2} - I_{L1}) = I_L - \frac{1}{4} \cdot (I_{Lpp2} - I_{Lpp1}) \qquad (10)$$

$$I_{L2} = I_L + \frac{1}{2} \cdot (I_{L2} - I_{L1}) = I_L + \frac{1}{4} \cdot (I_{Lpp2} - I_{Lpp1}) \qquad (11)$$

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DC balance with current signal injection

December 2012

And now to the calculation of Im.

$$\frac{\delta + \Delta\delta}{\delta - \Delta\delta} = \frac{\dfrac{Vin}{2} + \Delta V}{\dfrac{Vin}{2} - \Delta V} \qquad\qquad \frac{\delta + \Delta\delta}{\delta - \Delta\delta} = \frac{I_{L2} + Im}{I_{L1} - Im} \qquad\qquad (12)$$

The left hand part of (12) states that average voltage over Lm is zero. It is identical to (2).
The right hand part states that the net current flow into the capacitor midpoint is zero (hatched areas 1 and 2 in figure 8 must be the same).

Using only the right hand sides we have
$$\frac{\dfrac{Vin}{2} + \Delta V}{\dfrac{Vin}{2} - \Delta V} = \frac{I_{L2} + Im}{I_{L1} - Im} \qquad\qquad (13)$$

Solving for Im gives
$$Im = \frac{\Delta V}{Vin}\cdot\left(I_{L2} + I_{L1}\right) - \frac{1}{2}\cdot\left(I_{L2} - I_{L1}\right) \qquad\qquad (14)$$

Now we insert I_{L1} and I_{L2} from (10) and (11) in (14), and then insert (7):

$$Im = \Delta V\cdot\left(2\cdot\frac{I_L}{Vin} - \frac{1}{2}\cdot\frac{T}{L}\cdot\delta^2 \right) \qquad\qquad (15)$$

From (15) we can see that transformer magnetizing current is the difference between a term proportional to power (I_L) and a term inversely proportional to the output inductor. In most cases Im has the same sign as ΔV (see figure 8) but if L is small enough (high ripple current), Im can become zero or change sign. In figure 8 this means that the Im-blocks adding to and subtracting from inductor current will shift sign if there is a high ripple current relative to DC current.

At long last we are ready to continue with equation (1).

$$slope = \frac{\Delta y}{\Delta x} = \frac{2\cdot Im + \left(I_{Lpp2} - I_{Lpp1}\right)}{2\cdot\Delta\delta\cdot T} \qquad\qquad (16)$$

Inserting (15), (7) and (3) yields

$$slope = \frac{1}{2}\cdot\left(\frac{P\cdot Vin}{T\cdot Vo^2} + \frac{Vo}{L} \right) \qquad\qquad (17)$$

In (17) we have used that duty cycle $\delta = Vo / (0,5\cdot Vin)$ and power $P = I_L\cdot Vo$.

This result is much simpler than anybody could have expected. Let's discuss the result.

The slope unit is [A/second]. It expresses how much or how fast the peak current (turn-off current) must be reduced pr. time during a switching pulse, to stay at critical stability. In other words the minimum control slope to get a stable and controllable half bridge. It is the downslope of the peak current control signal in figure 8.

The first term is proportional to power and input voltage so the worst case is maximum power and maximum input voltage. The second term is independent on power and input voltage but it is inversely proportional to output inductor value. The second term is equal to the inductor current downslope. The two terms add, in contrary to the two terms in (15).

It is well known that a slope is also needed to prevent subharmonic oscillation if duty cycle becomes > 50%. That is known as "slope compensation". But the criteria (17) is completely different from that, and also applies if δ < 50%. Equation (17) requires much more slope than we need to prevent subharmonic oscillation.

In a real half bridge there is a transformer with a primary to secondary turns ratio $N = Np/Ns$. The control is done in a voltage comparator circuit, not in the power circuit. As illustrated in figure 7, the control circuit works with a voltage signal V_I equivalent to the numeric primary current. The pulse width is derived by comparing V_I to a DC feedback signal Vea minus a ramp voltage Vpp. The same method, adding a ramp to the numeric current signal, is

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page 8 of 11

Half bridge converter
DC balance with current signal injection

December 2012

used in full bridge converters to prevent subharmonic oscillation but the full bridge converter does not suffer from the "tilting" problem.

Equation (17) can easily be transformed to show how the minimum voltage control slope in a real half bridge must be calculated. Transforming secondary quantities to the primary side (as if the output was $N \cdot V_o$) is done by replacing V_o by $N \cdot V_o$ and L by $N^2 \cdot L$.

Transforming from current in the power part to an equivalent voltage signal is done by multiplying (17) by R_{sens}. R_{sens} can be a real resistor somewhere in the primary part, or more conveniently the transfer gain of a current transformer [V/A]. The required control ramp voltage slope then becomes:

$$V_{slope} > \frac{1}{2} \cdot \left[\frac{P \cdot V_{in}}{T \cdot (N \cdot V_o)^2} + \frac{V_o}{N \cdot L} \right] \cdot R_{sens} \tag{18}$$

If the control ramp has fixed slope and a period T, then the minimum required ramp peak-peak voltage becomes

$$V_{pp} = V_{slope} \cdot T \tag{19}$$

Alternatively, in a half bridge controlled by a known and fixed control ramp V_{pp}, (18) and (19) can be re-shaped to tell us a maximum allowed value of R_{sens}, i.e. a maximum allowed current signal injection, to maintain stability:

$$R_{sens} < \frac{2 \cdot V_{pp}}{\dfrac{P \cdot V_{in}}{(N \cdot V_o)^2} + \dfrac{V_o \cdot T}{N \cdot L}} \tag{20}$$

Benefits of current signal injection

The interesting conclusion is that, in contrary to the generally accepted assertion, it is possible to feed a certain amount of current signal into the pulse width modulator in a transformer coupled half bridge converter, and still maintain a stable balance in the half bridge.

Compared to a pure VMC controlled half bridge, the effect of just a tiny current signal injection can be more beneficial than you think. A VMC controlled half bridge has a 2nd order power stage transfer function with two complex poles, like a VMC controlled buck converter. It has a clear resonance frequency with a gain peak, above which the phase lag suddenly jumps close to 180 degrees. It is possible to properly compensate the feedback loop of a VMC controlled converter but it requires an error amplifier with a phase boost at the right frequency to counteract the 180 degrees in the power stage, known as a "type 3 compensator". This circuit can be delicate and intolerant to parameter variations.

By injecting a little current signal, the complex double pole is heavily damped, the resonance top vanishes and the phase lag increases much more gradually with frequency. That allows the feedback loop to be compensated better and with a simpler network, and the result is a power supply which is more robust against parameter variations.

Additionally, current signal injection reduces any tendency towards out-of-control magnetizing current, for instance if the load is pulsating at a frequency close to the switching frequency.

I will now give an example to show the persuasive effect of current signal injection.

Comparative example

In the example the following values are used:

Transformer turns ratio $N = 1{:}1$
Ouput inductor $L = 100\mu H$
Output capacitor $C_o = 100\mu F$ with ESR of $0{,}2\Omega$
Input voltage $V_{in} = 300V$
Output voltage $V_{out} = 120V$
Switching frequency (primary switches) $F = 100\ kHz$

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Half bridge converter
DC balance with current signal injection

December 2012

Output inductor current for this converter at 500 watt, at the selected operating conditions, is shown in figure 9.
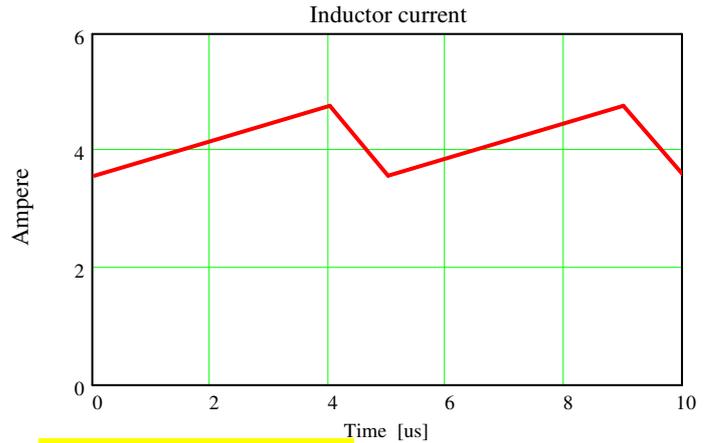
Mode = "continuous current"

Figure 9 Inductor current

Figure 10 shows calculated power stage gain
with half of the allowed current signal injection. You should not go much further than that because the calculated max. current signal injection is where the half bridge balance becomes unstable.

Power stage gain is defined as AC output current into the output capacitor C_o (with switching frequency ripple filtered out) versus small signal AC control voltage (V_{ea} in figure 7).
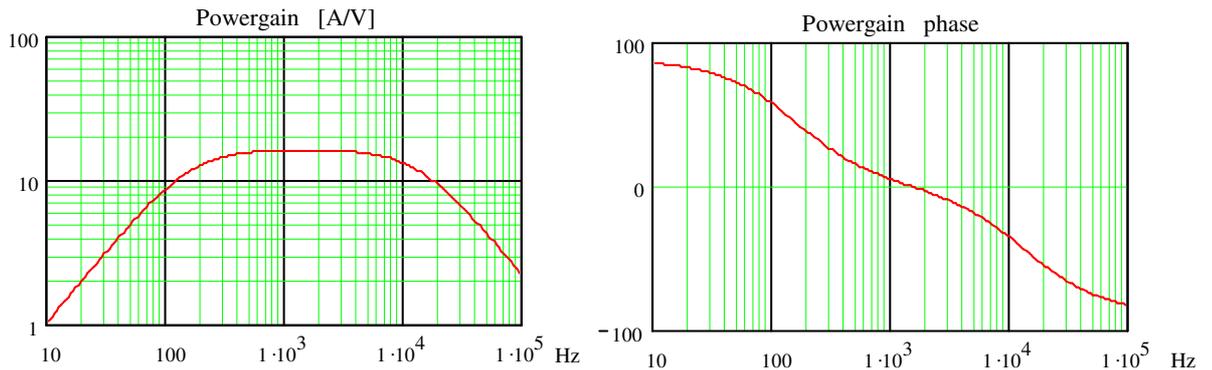
Figure 10

Current injection gain factor R_{sens} : $R_{sens} = 0.06$

Max. allowed R_{sens} for half bridge balance: $maxR_{sens} = 0.12$

Note the flat top on Powergain and gradual increase of phase delay.

Here is what it looks like if there is no current signal injection at all (pure VMC):
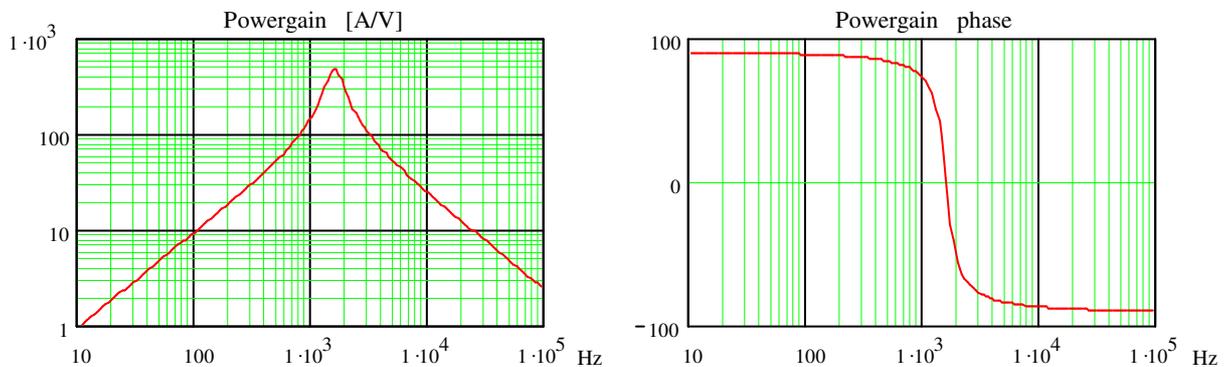
Figure 11

This is the well known LC resonance characteristic from pure Voltage Mode Control. $f_{res} = \dfrac{1}{2\pi\sqrt{L \cdot Co}}$.

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DC balance with current signal injection

December 2012

Figure 12 left: Total open loop gain with half of max. allowed current injection.

Right: Step load response with closed loop.

Open loop gain [dB]

Open loop phase [degrees]

Test frequency : $Fo \equiv 250$ [Hz]
Current step : $Istep \equiv 1$ [A]

Voltages at step load

Output step load response

Currents at step load

Load current step
Average inductor current in L
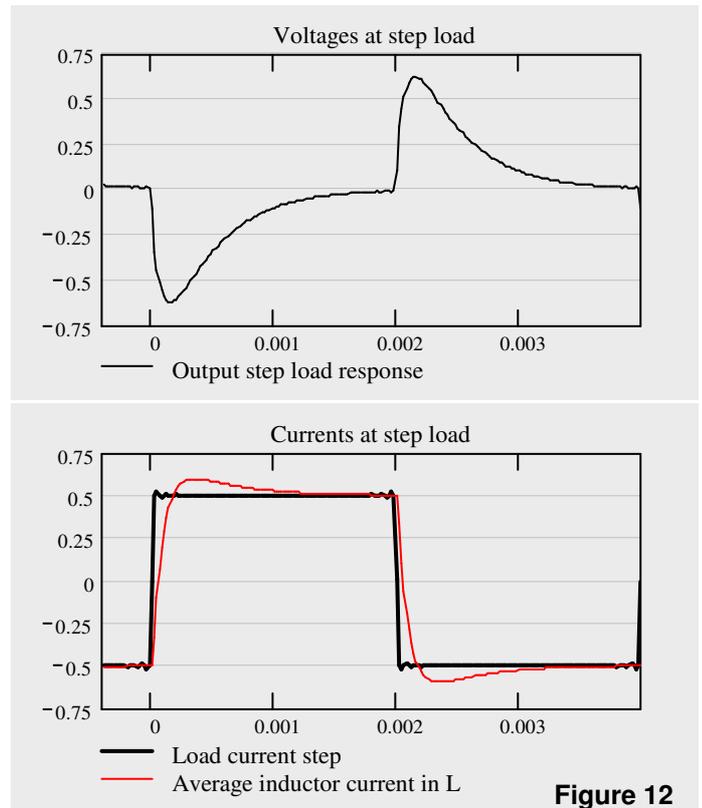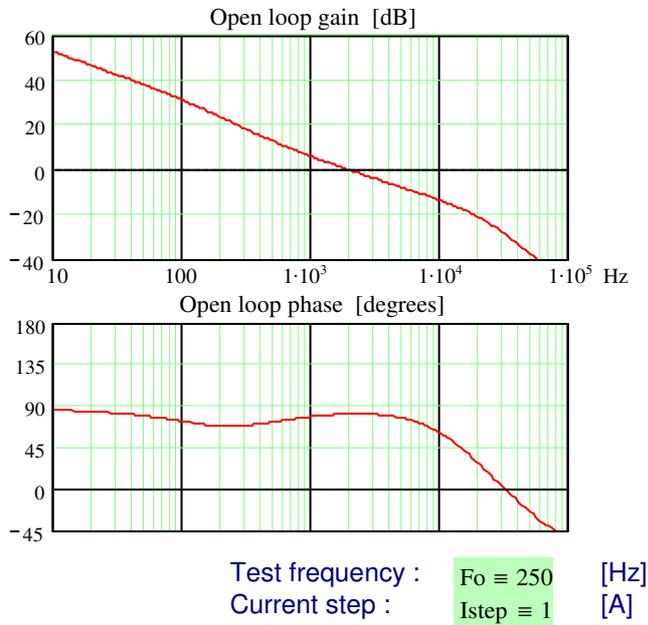
Figure 12

Figure 13 left: Total open loop gain with no current injection (pure VMC).

Right: Step load response showing ringing at the zero dB frequency 7kHz (not at the LC resonance frequency 1,5kHz !).

Open loop gain [dB]

Open loop phase [degrees]

Test frequency : $Fo \equiv 250$ [Hz]
Current step : $Istep \equiv 1$ [A]

Voltages at step load

Output step load response

Currents at step load

Load current step
Average inductor current in L

Figure 13

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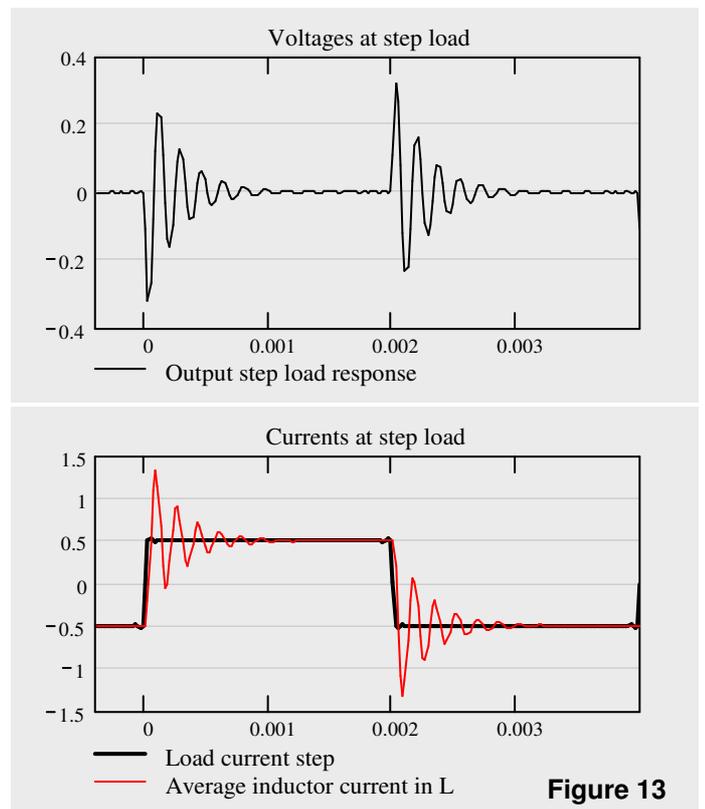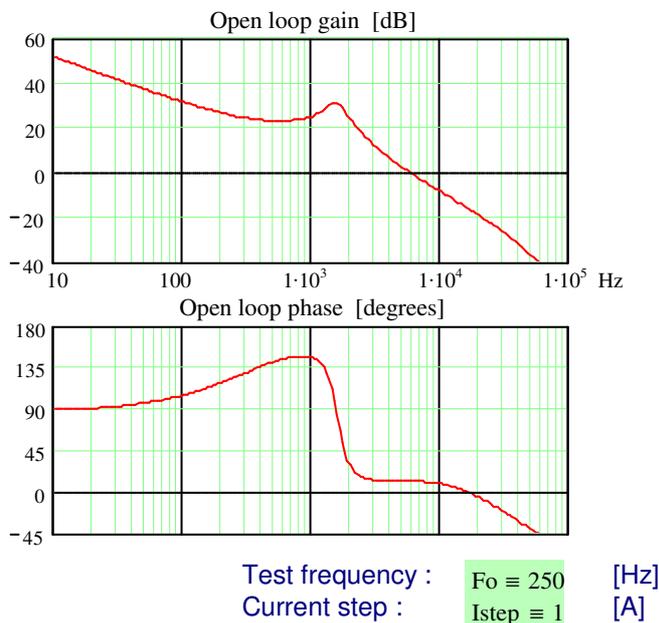
Half bridge converter
DC balance with current signal injection

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Figure 10 + 12 are with current signal injection, figure 11 + 13 are without.
The difference in feedback loop characteristics speaks for itself. Current signal injection, even with less than allowed size, changes the complex double pole to something much more easy to handle.

The compensation network is the same in the two examples in order to demonstrate the important differences. Note that only the middle frequency part of the gain and phase are influenced but this is exactly where the gain and phase shapes are important.

In each of the two cases we can or must optimize the compensation network further. In the first case, gain can be increased to reduce the voltage jumps after a step load: 6 - 10dB gain increase would do very well.
In the latter case, a "type 3 network" must be used to increase the phase margin and get rid of the ringing. However that converter is less tolerant to parameter variations.

Postscript

I have used small amounts of current signal injection in my designs of half bridge converters for many years, mainly because of its merits in feedback loop design. Any mixture of Voltage Mode and Current Mode Control has long been part of my feedback loop calculators. But until the writing of this article I have had no idea of how much current signal injection a half bridge can tolerate before the DC balance is lost.
The present article is based on some geometric and mathematical thinking but before that, a lot of simulations were done in an ideal half bridge with variable component values. Without help from simulations it is very easy to think wrong. After deriving the equations, simulation was again used to check the results with some typical component values and good agreement was found.
The results are now incorporated into my half bridge loop calculator, and the graphs in the previous pages are printouts from that.

However, the assumptions done in the derivation are not always completely true. Simulations showed that if, for instance, the magnetizing inductance of the transformer is very large – larger than realistic – then some low frequency oscillations appear in the midpoint balance, even though the condition for current signal injection in this article is met. During this oscillation there is low frequency AC current in the magnetizing inductance which is delayed after the capacitor midpoint AC voltage. One assumption I have done is that magnetizing current will flow if there is a voltage imbalance. But with a large enough magnetizing inductance, current must wait some time before it can flow, and that seems to spoil the validity of my model. However, with realistic values of magnetizing inductance, the model seems to be true.

Large values of half bridge capacitors, on the contrary, do not seem to cause oscillations or other deviations from the model's predictions.

Chaotic behaviour was also seen in many of the simulations which, I believe, can never be described or understood by a simple model. Therefore I encourage you to use my equations to design better half bridges, but use them as a guide and always check that your half bridge is not close to a balance problem. I practice you can do this by experimentally doubling your current signal injection at maximum load and maximum input voltage and verifying that the DC balance of your half bridge does still not tilt.

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